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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/749,590	12/28/2000	Fumio Ohtake	001752	4831

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EXAMINER

MAI, ANH D

ART UNIT PAPER NUMBER

2814

DATE MAILED: 12/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/749,590

Applicant(s)

OHTAKE ET AL.

Examiner

Anh D. Mai

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 02 October 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) 11-17 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10, 18 and 19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 02 October 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION*****Amendment***

1. Amendment filed October 2, 2002 has been entered as Paper No. 11. Claims 1 and 2 have been amended. Claims 18 and 19 have been added. Claims 1-19 are pending. Claims 11-17 have been withdrawn.

***Drawings***

2. The corrected or substitute drawings were received on October 2, 2002. These drawings are acceptable.

***Claim Rejections - 35 USC § 103***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 2, 5, 6, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over K. Kasai et al. *W/WN<sub>x</sub>/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs* (cited previously) in view of Jeng et al. (U.S. Patent No. 5,877,074).

With respect to claims 1 and 2, Kasai teaches a semiconductor device substantially as claimed including:

a pair of impurity diffused regions formed in a silicon substrate, spaced from each other;  
and

a gate electrode formed above the silicon substrate between the pair of impurity diffused regions with a gate insulation film interposed therebetween, the gate electrode being formed of a first polycrystalline silicon film formed on the gate insulation film, a second polycrystalline silicon film formed on the first polycrystalline silicon film and having crystal grain boundaries

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which are discontinuous to the first polycrystalline silicon film, and a metal nitride film ( $WN_x$ ) formed on the second polycrystalline silicon film, and a metal film (W) formed on the metal nitride film. (See Fig. 2).

Thus, Kasai is shown to teach all the features of the claim with the exception of the second polycrystalline silicon film having a thickness thinner than that of the first polycrystalline silicon film.

However, Jeng in a semiconductor device teaches: a gate electrode formed above the silicon substrate (11) with a gate insulation film (12) interposed therebetween, the gate electrode being formed of a first polycrystalline silicon film (31) formed on the gate insulation film (12), a second polycrystalline silicon film (32) formed on the first polycrystalline silicon film (31) having a thickness thinner than that of the first polycrystalline silicon film (31). (See Fig. 5).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the second polycrystalline silicon film of Kasai to the thickness as taught by Jeng to prevent impurity atoms from penetration during the formation of the metal layer (W).

Regarding the second polycrystalline silicon film, the  $\alpha$ -Si of the references are subjected to a high temperature anneal, thus, crystallized, hence polycrystalline silicon. Further, since the  $\alpha$ -Si is formed at a lower temperature than that of the polysilicon (first) layer, thus, the grain size is differed than that of polysilicon, therefore, the crystal grain boundary of the two layer are discontinuous. The subject matter is well known in the art.

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With respect to claims 5 and 6, the first polycrystalline silicon film of Kasai further includes boron.

With respect to claims 18 and 19, the second polycrystalline silicon film (32) of Jeng having a thickness that includes the upper limit (20 nm) of the claims.

Further, within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum thickness of the second polycrystalline silicon film. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation".

4. Claims 3, 4 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai et al. and Jeng '074 as applied to claims 1 and 2 above, and further in view of Tsukamoto (U.S. Pub. No. 2001/0000629) (cited previously).

With respect to claims 3 and 4, Kasai and Jeng teaches a gate electrode formed above the semiconductor substrate including the second polycrystalline silicon film formed on the first polycrystalline silicon film.

Thus, Kasai and Jeng are shown to teach all the features of the claim with the exception of explicitly disclosing an oxide film formed between the first and second polycrystalline silicon films.

However, Tsukamoto teaches a native oxide film (20) is formed between the first (6) and second (7) polycrystalline silicon film so that the grain size of the second polycrystalline silicon film (7) can become large. (See Fig. 6).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form an oxide film between the first and second polycrystalline silicon films of Kasai as taught by Tsukamoto to suppress fluctuation in the threshold voltage  $V_{th}$ .

With respect to claims 7 and 8, the first (6) and second (7) polycrystalline silicon film of Tsukamoto are further doped with boron. Further, the native oxide layer (20) formed between the two polycrystalline silicon films (6, 7) functions as impurities diffusion blocker (suppress fluctuations in the threshold voltage  $V_{th}$  caused by mutual diffusion of the impurities) and following an anneal step, the impurities are known to segregate toward the upper surface, therefore, the boron concentration in the first polycrystalline silicon film (6) near the interface between the first polycrystalline silicon film (6) and the second polycrystalline silicon film (7) is higher than boron concentration in the second polycrystalline silicon film (7) near an interface between the first polycrystalline silicon film (6) and the second polycrystalline silicon film (7).

With respect to claims 9 and 10, the crystal grain size of the first polycrystalline silicon film (6) of Tsukamoto is smaller than that of the second polycrystalline silicon film (7).

### ***Response to Arguments***

5. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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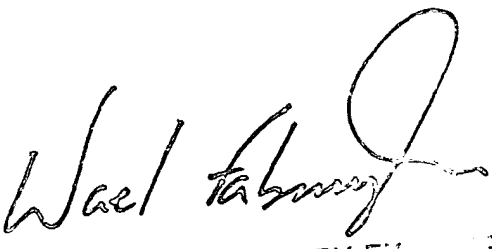
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M  
December 10, 2002

  
Wael Fahmy  
PRIMARY EXAMINER